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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	14

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,597	ENGLIN ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed March 22, 2004 in response to PTO Office Action mailed December 22, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-25 have been presented for examination in this application. In response to the last Office Action, claims 1, 6, 11 and 16-20 have been amended. No claims have been canceled. Claims 21-25 have been added. As a result, claims 1-25 are now pending in this application.

3. The rejection of claims 1-5 under 35 USC 112, first paragraph has been withdrawn due to the amendment filed March 22, 2004.

Response to Arguments

4. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 6, 7, 11, 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094).

As per claims 1 and 6, Kranich discloses a data processing system including a plurality of processors each directly coupled via a system memory bus [*processors 10-12 coupled to each other by memory bus 40*; Fig. 1], wherein a first processor of said plurality of processors contains a level one cache memory directly coupled to a level two cache memory which is directly coupled to a level three memory [*level 2 cache is operatively coupled to level 1 cache and higher level caches are operatively coupled to next lower level cache*; col. 3, lines 29-34; Fig. 1]; said level two cache memory containing cache storage and tag storage [*level 2 cache 30 contains data array 205 and tag array 203*; Fig. 3], and containing a circuit for SNOOPing said system memory bus [*the highest level cache includes a means for monitoring the shared memory bus*; col. 3, lines 43-44].

However, Kranich does not specifically teach the improvement comprising a first dedicated path between said system bus and said cache storage and a second dedicated path between said system bus and said tag storage as recited in the claim.

Kumar discloses a data processing system for reducing cache latency wherein the improvement comprises a first dedicated path between a system bus and a cache

storage [*front side bus 190 communicates with L2 data array by means of line connected to way predictor 150*; Fig. 7], and a second dedicated path between a system bus and a tag storage [*front side bus 190 communicates with L2 tag array 135 by means of snoop queue line*; *Fig.* 7], in order for the microprocessor to directly access the cache tag array without accessing the external bus during a lookup [col. 5, lines 24-32], in order for the microprocessor to directly access the cache tag array without accessing the external bus during a lookup (col. 5, lines 24-32).

Note that Kumar further discloses that the combination of the cache tag array 55 and cache data array 60 in Fig. 3 could serve as a secondary cache as detailed in col. 6, lines 1-10.

Since the technology for implementing a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path was well known in the art and since a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path reduces cache latency by allowing the microprocessor to directly access the cache tag array without accessing the external bus during a lookup, an artisan would have been motivated to use a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path in the system of Kumar. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path because it was well known to reduce

cache latency by allowing the microprocessor to directly access the cache tag array without accessing the external bus during a lookup as taught by Kumar.

As per claim 7, Kranich discloses a data request transferred from said level one cache memory to a level two cache memory [*if level 1 cache does not have the requested address, the level 2 cache will next try to service the processor address request*; col. 4, lines 41-43].

As per claim 11, Kranich discloses a method of maintaining validity of data within a level one cache memory of a processor having a level one tag memory [*level one tag array 213 of level one cache 20*; Fig. 2] directly coupled to a level two cache memory containing a tag memory and a data memory [*level 1 cache 20 is directly coupled to level 2 cache 30*; Fig. 1; *level 2 tag array 203 of level 2 cache 30*; Fig. 2] wherein said level two cache memory is directly coupled to a system memory bus [*level 2 cache 30 is directly coupled to bus 40*; Fig. 1] comprising: formulating a SNOOP request [*monitoring is performed by a snooping process*; col. 2, lines 6-7]; presenting said SNOOP request on said system memory bus to said level two cache memory [*the level 2 cache snoops the external accesses over the shared memory bus*; col. 2, lines 14-15]; routing said SNOOP request directly to said tag memory via said second dedicated path [*the snoop process includes examines the tag array by means of snoop queue line*; Fig. 7; col. 2, lines 6-10]; processing said SNOOP request [*the snoops results in a level 2 cache hit*; col. 2, lines 21-29].

However, Kranich does not specifically teach a system memory bus coupled to said data memory via a first dedicated path, and to said tag memory via a second dedicated path as recited in the claim.

Kumar discloses a system memory bus coupled to a data memory via a first dedicated path [*front side bus 190 communicates with L2 data array by means of line connected to way predictor 150*; Fig. 7], and to a tag memory via a second dedicated path [*front side bus 190 communicates with L2 tag array 135 by means of snoop queue line*; *Fig.* 7], in order for the microprocessor to directly access the cache tag array without accessing the external bus during a lookup (col. 5, lines 24-32). Since the technology for implementing a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path was well known in the art and since a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path reduces cache latency by allowing the microprocessor to directly access the cache tag array without accessing the external bus during a lookup, an artisan would have been motivated to use a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path in the system of Kumar. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path because it was well known to reduce cache latency by allowing the microprocessor to directly access the cache tag array without accessing the external bus during a lookup as taught by Kumar.

As per claim 16, Kranich discloses an apparatus comprising:

a. Executing means for executing program instructions [*processors 10-12*; Fig. 1];

b. Level one caching means directly coupled to said executing means for level one caching data [*level 1 caches 20-22 are directly coupled to processors 10-12*; Fig. 1];

c. Requesting means directly coupled to said executing means and said level one caching means for requesting a data element if said executing means requires requesting of said data element and said level one caching means does not contain said data element [*level 1 cache controller 211*; Fig. 2];

d. Level two caching means directly coupled to said requesting means for level two caching [*level 2 cache 30-32 directly coupled to level 1 caches 20-22 which contain controller 211*; Fig. 1];

e. Storing means located within said level two caching means for storing level two caching data [*data array 205*; Fig. 2];

f. Maintaining means located within said level two caching means for maintaining level two tags [*level 2 tag array 203 of level 2 cache 30*; Fig. 2];

g. Snooping means directly coupled to said maintaining means for directly snooping said level two tags [*highest level cache includes a means for monitoring the shared memory bus;* col. 3, lines 43-44; *monitoring is performed by a snooping process*; col. 2, lines 6-7; *the snoop process includes examines the tag array*; col. 2, lines 6-10].

However, Kranich does not specifically teach that the snooping means is directly coupled via a dedicated path to the maintaining means as recited in the claim.

Kumar discloses a front side bus 190 communicates with L2 tag array 135 directly connected to snoop queue line 165 as shown in *Fig.* 7, in order for the microprocessor to directly access the cache tag array without accessing the external bus during a lookup (col. 5, lines 24-32). Since the technology for implementing a snooping means directly coupled via a dedicated path to a maintaining means was well known in the art and since a snooping means directly coupled via a dedicated path to a maintaining means reduces cache latency by allowing the microprocessor to directly access the cache tag array without accessing the external bus during a lookup, an artisan would have been motivated to use a snooping means directly coupled via a dedicated path to a maintaining means in the system of Kumar. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a snooping means directly coupled via a dedicated path to a maintaining means because it was well known to reduce cache latency by allowing the microprocessor to directly access the cache tag array without accessing the external bus during a lookup as taught by Kumar.

As per claim 21, Kranich discloses a data processing system having a plurality of processors comprising:

a main memory [*main memory 50*; Fig. 1]; a system bus responsively coupled to said main memory [*bus 40 coupled to main memory 50*; Fig. 1]; a plurality of cache memory units wherein each of said plurality of cache memory units is dedicated to a different one of said plurality of processors [*caches 20-22 and caches 30-32 coupled to processors 10-12*;

Fig. 1]; a plurality of cache data storage units wherein each of said plurality of cache data storage units is located in a different one of said plurality of cache memory units [*data arrays 205 and 215 in each of said level 1 and level 2 caches*; Fig. 2]; a plurality of tag storage units wherein each of said plurality of tag storage units is located in a different one of said plurality of cache memory units [*tag arrays 203 and 213 in each of said level 1 and level 2 caches*; Fig. 2];

a plurality of first direct paths wherein each of said plurality of first direct paths directly couples a different one of said plurality of cache data storage units to said system bus; and a plurality of second direct paths wherein each of said plurality of second direct paths directly couples a different one of said plurality of tag storage units to said system bus.

However, Kranich does not specifically teach a plurality of first direct paths between said system bus and said cache storage and a second direct path between said system bus and said tag storage as recited in the claim.

Kumar discloses a data processing system for reducing cache latency wherein the improvement comprises a first direct path between a system bus and a cache storage [*front side bus 190 communicates with L2 data array by means of line connected to way predictor 150*; Fig. 7], and a second direct path between a system bus and a tag storage [*front side bus 190 communicates with L2 tag array 135 by means of snoop queue line*; *Fig.* 7], in order for the microprocessor to directly access the cache tag array without accessing the external bus during a lookup [col. 5, lines 24-32], in order for the microprocessor to

directly access the cache tag array without accessing the external bus during a lookup (col. 5, lines 24-32).

Note that Kumar further discloses that the combination of the cache tag array 55 and cache data array 60 in Fig. 3 could serve as a secondary cache as detailed in col. 6, lines 1-10.

Since the technology for implementing a system memory bus coupled to a data memory via a first direct path, and to a tag memory via a second direct path was well known in the art and since a system memory bus coupled to a data memory via a first direct path, and to a tag memory via a second direct path reduces cache latency by allowing the microprocessor to directly access the cache tag array without accessing the external bus during a lookup, an artisan would have been motivated to use a system memory bus coupled to a data memory via a first direct path, and to a tag memory via a second direct path in the system of Kumar. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a system memory bus coupled to a data memory via a first direct path, and to a tag memory via a second direct path because it was well known to reduce cache latency by allowing the microprocessor to directly access the cache tag array without accessing the external bus during a lookup as taught by Kumar.

7. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094) and Stevens et al. (US5,426,765).

As per claims 2 and 8, Kranich discloses a control logic directly coupled to a cache storage and a tag storage [*cache controller 201 coupled to tag array 203 and cache 30*; Fig. 2]. However, the combination of Kranich and Kumar discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Kumar do not specifically teach a control logic which provides the highest priority for a SNOOPing as recited in the claims.

Stevens discloses a control logic which provides the highest priority for a SNOOPing, in order to provide minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency (col. 4, lines 15-32). Since the technology for implementing a control logic which provides the highest priority for a SNOOPing was well known and since a control logic which provides the highest priority for a SNOOPing provides minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency, an artisan in the art would have been motivated to use a control logic which provides the highest priority for a SNOOPing in the system of Kranich and Kumar. Thus, it would have been obvious to one of ordinary skill in the art to modify the system of Kranich and Kumar because a control logic which provides the highest priority for snooping benefits by providing

minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency as taught by Stevens.

8. Claims 3-5, 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094) and Stevens et al. (US5,426,765) and further in view of Duncan (US6,353,877).

As per claim 3, the combination of Kranich and Kumar and Stevens discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Kumar and Stevens do not specifically teach do not specifically teach a level two cache comprising a duplicate tag memory as recited in the claim.

Duncan discloses a level two cache comprising a duplicate tag store, in order to facilitate a determination as to the contents of the other caches of the processor (*all caches communicate with duplicate tag store 54*; Fig. 2; col. 7, line 30). Since the technology for implementing a duplicate tag store was well known and since a duplicate tag store benefits by maintaining cache coherency by facilitating a determination as to the contents of the other caches of the processor, an artisan would have been motivated to use a level two cache comprising a duplicate tag store in the system of Kranich and Kumar and Stevens. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Kumar and Stevens and Duncan before him at the

time the invention was made, to modify the system of Kranich and Kumar and Stevens because a duplicate tag store benefits by maintaining cache coherency by facilitating a determination as to the contents of the other caches of the processor as taught by Duncan.

As per claims 4 and 22, Kranich discloses said plurality of processors further comprises a plurality of instruction processors [*processors make requests*; col. 4, lines 34-35].

As per claim 5, Kumar discloses said level three memory further comprises a level three cache memory [*third level cache, L2*; col. 9, line 24; Fig.7].

As per claim 23, Kranich discloses at least one of said plurality of processors further comprises a dedicated level one cache memory [*level 1 caches 20-22 are directly coupled to processors 10-12*; Fig. 1].

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094) and Stevens et al. (US5,426,765) and further in view of Fu (US6,457,087).

As per claim 9, Kranich discloses a data processing system comprising a level one tag memory located within a level one cache memory [*tag array 213 in level 1 cache memory*; Fig. 2].

However, the combination of Kranich and Stevens discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Stevens do not specifically teach a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory.

Fu discloses a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within a level one tag memory [*L2 duplicate tag memory 232 contains duplicate tags for each data block in L2 which contains data that is stored in L1*; Fig. 5C] in order to provide an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Fu before him at the time the invention was made, to modify the system of Kranich and Stevens to include a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory because it was well known to provide an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system [col. 31, lines 11-16] as taught by Fu.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094) and Stevens et al. (US5,426,765) and Fu (US6,457,087) and further in view of Duncan (US6,353,877).

As per claim 10, the combination of Kranich and Kumar and Stevens and Fu discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Kumar and Stevens do not specifically teach a SNOOP request directly coupled to a duplicate tag memory as recited in the claim.

Duncan discloses a SNOOP request directly coupled to a duplicate tag memory [*bus control logic 58 which receives the snoop requests is coupled to duplicate tag 54*; Fig. 2], which benefits by monitoring the bus to determine if the requested block is present in the respective caches (col. 8, lines 10-15). Since the technology for implementing a SNOOP request directly coupled to a duplicate tag memory was well known in the art and since a SNOOP request directly coupled to a duplicate tag memory benefits by monitoring the bus to determine if the requested block is present in the respective caches, an artisan would have been motivated to use a SNOOP request directly coupled to a duplicate tag memory in the combination of Kranich and Kumar and Stevens and Fu. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Kumar and Stevens and Fu and Duncan before him at the time the invention was made, to modify the system of Kranich and Kumar and Stevens and Fu because coupling snoop request to a duplicate tag memory benefits in monitoring the bus by determine if the requested block is present in the respective caches as taught by Duncan.

11. Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765).

As per claims 12 and 17, Kranich discloses a data request transferred from said level one cache memory to a level two cache memory [*if level 1 cache does not have the requested address, the level 2 cache will next try to service the processor address request*; col. 4, lines 41-43].

However, Kranich does not specifically teach a control logic which provides the highest priority for a SNOOPing as recited in the claims.

Stevens discloses a control logic which provides the highest priority for a SNOOPing [col. 4, lines 23-32], in order to provide minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens before him at the time the invention was made, to modify the system of Kranich because a control logic which provides the highest priority for snooping benefits by providing minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency [col.4, lines 15-20] as taught by Stevens.

12. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and further in view of Fu (US6,457,087).

As per claim 13, the combination of Kranich and Stevens discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Stevens do not specifically teach a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory.

Fu discloses a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within a level one tag memory [*L2 duplicate tag memory 232 contains duplicate tags for each data block in L2 which contains data that is stored in L1*; Fig. 5C] in order to provide an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Fu before him at the time the invention was made, to modify the system of Kranich and Stevens to include a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory because it was well known to provide an improved cache coherency in the system by

allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system [col. 31, lines 11-16] as taught by Fu.

13. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and Fu (US6,457,087) and further in view of Duncan (US6,353,877).

As per claims 14 and 15, the combination of Kranich and Stevens and Fu discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Stevens do not specifically teach routing said SNOOP request to a duplicate tag memory and processing said SNOOP request regarding said duplicate tag memory as recited in the claims.

Duncan discloses routing said SNOOP request to a duplicate tag memory [col. 8, lines 11-15]; processing said SNOOP request regarding said duplicate tag memory [col. 8, lines 11-20] to determine if the requested block is present in the respective caches.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Fu and Duncan before him at the time the invention was made, to modify the system of Kranich and Stevens and Fu because routing and processing snoop request to a duplicate tag memory benefits in monitoring the bus by determine if the requested block is present in the respective caches [col. 8, lines 10-15] as taught by Duncan.

14. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and Kumar et al (US6,247,094).

As per claim 18, Kranich discloses means directly coupled to said level two caching means for bussing system memory data [shared memory bus 40; Fig. 1]; means directly coupled to said bussing means for interfacing said bussing means directly to said storing means [*level 2 cache is directly coupled to bus 40*; Fig. 1].

However, the combination of Kranich and Stevens does not specifically teach means directly coupled to said bussing means for interfacing said bussing means directly to said maintaining means as recited in the claim.

Kumar discloses a data processing system for reducing cache latency wherein means directly coupled to a bussing means for interfacing said bussing means directly to a maintaining means [*front side bus 190 communicates with L2 tag array 135 by means of snoop queue line*; *Fig.* 7], in order for the microprocessor to directly access the cache tag array without accessing the external bus during a lookup [col. 5, lines 24-32].

Note that Kumar discloses that the combination of the cache tag array 55 and cache data array 60 in Fig. 3 could serve as a secondary cache as detailed in col. 6, lines 1-10.

Therefore, it would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Kumar before him at the time the invention was made, to modify the system of Kumar because directly accessing a maintaining means benefits

with reduced cache latency so that the microprocessor to directly access the cache tag array without accessing the external bus during a lookup.

15. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and Kumar et al (US6,247,094) and further in view of Fu (US6,457,087).

As per claim 19, the combination of Kranich and Stevens and Kumar discloses the claimed invention as detailed above in the previous paragraphs. Kranich further discloses means located within said level one caching means for recording level one tags [*level 1 tag array 213*; Fig. 2]. However, Kranich and Stevens and Kumar do not specifically teach means located within said level two caching means and directly coupled to said recording means for duplicating said level one tags as recited in the claim.

Fu discloses means located within a level two caching means and directly coupled to a recording means for duplicating level one tags [*L2 duplicate tag memory 232 contains duplicate tags for each data block in L2 which contains data that is stored in L1*; Fig. 5C] in order to provide an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Kumar and Fu before him at the time the

invention was made, to modify the system of Kranich and Stevens and Kumar to include means located within a level two caching means and directly coupled to a recording means for duplicating level one tags because it was well known to provide an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system [col. 31, lines 11-16] as taught by Fu.

16. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and Kumar et al (US6,247,094) and Fu (US6,457,087) and further in view of Duncan (US6,353,877).

As per claim 20, the combination of Kranich and Stevens and Kumar and Fu discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Stevens and Kumar and Fu do not specifically teach means directly coupled to said bussing means and said duplicating means for snooping said duplicating means as recited in the claim.

Duncan discloses means directly coupled to said bussing means and said duplicating means for snooping said duplicating means [*bus control logic 58 which receives the snoop requests is coupled to duplicate tag 54*; Fig. 2; col. 8, lines 11-20] to determine if the requested block is present in the respective caches.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Fu and Duncan before him at the time the

invention was made, to modify the system of Kranich and Stevens and Fu because routing and processing snooping a duplicate means benefits in monitoring the bus by determine if the requested block is present in the respective caches [col. 8, lines 10-15] as taught by Duncan.

17. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094) and Stevens et al. (US5,426,765) and further in view of Duncan (US6,353,877) and Cohen et al (US5,692,152).

As per claim 24, the combination of Kranich and Kumar and Stevens and Duncan discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Kumar and Stevens and Duncan do not specifically teach a dedicated level one cache memory further comprises a read only instruction cache memory as recited in the claim.

Cohen discloses a processor having a private level one read-only instruction cache which holds instructions only to supply the maximum bandwidth of the processor's pipelines (col. 4, lines 50-53; col. 23, lines 20-26). Since the technology for implementing a read-only instruction cache was well known and since a read-only instruction cache supplies the maximum bandwidth of the processor's pipelines, an artisan would have been motivated to use a read-only cache in the combination of Kranich and Kumar and Stevens and Duncan. Thus, it would have been obvious to one

of ordinary skill in the art at the time the invention was made to implement a private read-only instruction cache because it was well known to supply the maximum bandwidth of the processor's pipelines as taught by Cohen.

As per claim 25, the combination of Kranich and Kumar and Stevens and Duncan discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Kumar and Stevens and Duncan do not specifically teach discloses a dedicated level one cache memory further comprises a read/write operand cache memory as recited in the claim.

Cohen discloses a dedicated level one cache memory comprising a read/write operand cache memory to supply the maximum bandwidth of the processor's pipelines (col. 4, lines 50-53; col. 23, lines 20-26). Since the technology for implementing a level one cache memory comprising a read/write operand cache memory was well known and since a level one cache memory comprising a read/write operand cache memory supplies the maximum bandwidth of the processor's pipelines, an artisan would have been motivated to use a level one cache memory comprising a read/write operand cache memory in the combination of Kranich and Kumar and Stevens and Duncan. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a level one cache memory comprising a read/write operand cache memory because it was well known to supply the maximum bandwidth of the processor's pipelines as taught by Cohen.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach multilevel cache memory and prioritizing snoop request over processor request, read-only level one cache and level one operand cache.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-

5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 30, 2004

Pierre M. Vital
Examiner
Art Unit 2188